Software-based Selective Voting for Dependable Coarse-Grained Reconfigurable Architectures against Soft Errors

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Abstract

Coarse-Grained Reconfigurable Architectures or CGRAs are drawing significant attention since they promise both performances with parallelism and flexibility with reconfiguration. CGRA is in general composed of grid-based PEs (Processing Elements) and each PE consists of a FU (Functional Unit) and a few registers. CGRA is a promising alternative as an accelerator since this simple architecture can improve the performance massively by executing application loop kernels on PEs in parallel with the inherent efficacy of power consumption [5]. Soft errors or transient faults are becoming a serious design concern in embedded systems including CGRAs since soft error rate is increasing exponentially as technology scaling [1]. As the popularity of CGRA usages is increasing on many embedded applications such as human health systems, automobiles, airplanes, and data server systems [3], a single soft error may lead to catastrophic consequence, and even a human life. In order to make CGRAs robust against soft errors, several hardware-based techniques have been proposed, but they are expensive in terms of area, energy, and performance. Most of hardware based techniques modify existing architectures to implement redundancy based DMR (Dual Modular Redundancy) [2] and TMR [4] and they incur high costs in every design aspect. On the other hand, a recently proposed software-based technique with TMR (Triple Modular Redundancy) implemented on CGRAs incurs extreme overheads in terms of runtime and energy consumption mainly due to expensive voting mechanisms for the outputs from the triplication of every operation [6]. In this talk, we present selective voting mechanisms for efficient modular redundancy techniques in the datapaths on CGRAs. Our techniques selectively vote the results at synchronous operations rather than every operation in order to reduce the expensive performance overhead from the software-based voting mechanism. We also present an optimization technique to further improve the runtime and the energy consumption by minimizing synchronous operations where voting mechanism needs to be applied. Our experimental results demonstrate that our selective voting based TMR technique with our optimization on CGRAs can improve the runtime by 41.0% and the energy consumption by 26.2% on average over benchmarks as compared to the recently proposed software-based TMR technique with the full voting. Further, our selective voting technique demonstrates the comparable fault coverage even though the number of votings is reduced as compared to TMR with the full voting. In order to analyze the fault coverage, we have implemented a framework for fault injection experiments. The average failure rate of full voting is 0.0025% and the average failure rate of selective voting 0.0030%. The difference of failure rate between two techniques is about 0.00056%p on average.

Categories and Subject Descriptors B.8.1 [*Performance and Reliability*]: Reliability, Testing, and Fault-Tolerance; C.4 [*Computer Systems Organization*]: Performance of Systems-*Fault tolerance*; D.3.4 [*Programming Languages*]: Processors-*Code generation; Compilers; Optimization*

General Terms Design, Performance, Reliability

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